L Number	Hits	Search Text	DB	Time stamp
1	838	dummy with (patterns or conductors)	USPAT; US-PGPUB	2002/06/27 13:13
2	144	(dummy with (patterns or conductors)) and dielectric and (trenches or grooves or openings or holes)	USPAT; US-PGPUB	2002/06/27 13:13
3	77	((dummy with (patterns or conductors)) and dielectric and (trenches or grooves or openings or holes)) and @ad<=19980831	USPAT; US-PGPUB	2002/06/27 13:13
4	985	dummy with (patterns or conductors)	EPO; JPO; DERWENT; IBM_TDB	2002/06/27 13:13
5	6	(dummy with (patterns or conductors)) and dielectric and (trenches or grooves or openings or holes)	EPO; JPO; DERWENT; IBM_TDB	2002/06/27 13:14

CLIPPEDIMAGE= JP411265866A
PAT-NO: JP411265866A
DOCUMENT-IDENTIFIER: JP 11265866 A
TITLE: PLANARIZATION OF DAMASCENE METALLIC CIRCUIT PATTERN

PUBN-DATE: September 28, 1999

INVENTOR-INFORMATION:

NAME	COUNTRY
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NAME	COUNTRY
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SIEMENS AG	N/A

APPL-NO: JP11005128
APPL-DATE: January 12, 1999

INT-CL_(IPC): H01L021/304

ABSTRACT:
PROBLEM TO BE SOLVED: To polish efficiently a work covered with a metal layer applying a damascene method by a method wherein a wafer covered with the metal layer is polished unit the metal layer is stopped leaving on the outside of a desired circuit **pattern** and the outside of an arbitrary **dummy** circuit **pattern**.

SOLUTION: **Opening** parts 15a, 15b, 15c and 15d for interconnecting **opening** parts are formed in a silicon dioxide **dielectric** layer 14 laminated on a silicon substrate 13, a metal layer 16, which is extended from the surface of the layer 14 to the surface of the silicon wafer 13, is covered on the upper surface of the layer 14 and the **opening** parts 15a to 15d and dummy **opening** parts 20 are filled with the layer 16, but a metallization on the

surface of a region 17 is
evenly executed. The metallized wafer is placed on a chemical polishing
machine using a well-know means and the layer 16 is removed up to the surface
of the layer 14. The surface of the remaining layer 14, which is shown at the
end parts 14a and 14b on both sides of the layer 14, is substantially formed
horizontally extending over the whole region 17 of chips.

DERWENT-ACC-NO: 2001-059432
DERWENT-WEEK: 200107

TITLE: CMP uniformity increasing method, obtaining consistent density and distribution of active regions on one chip

INVENTOR: GUO, J; JIAN, S ; LI, T ; LIAU, W

PATENT-ASSIGNEE: UNITED MICROELECTRONICS CORP[UNMIN]

PRIORITY-DATA: 1998TW-0115165 (September 11, 1998)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
TW 388932 A	May 1, 2000	N/A	015	H01L 021/304

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
TW 388932A	N/A	1998TW-0115165	September 11, 1998

INT-CL_(IPC): H01L021/304

ABSTRACTED-PUB-NO: TW 388932A
BASIC-ABSTRACT: NOVELTY - Method comprises providing semiconductor substrate at least including first and second circuit regions. Separately forming plurality of **trenches** in circuit regions, **trenches** having various sizes in circuit regions. Separately forming **dummy pattern on trenches** having larger size through program analysis procedure, and forming **dielectric** layer covering substrate for planarization process by CMP.

USE - A method of increasing the uniformity of chemical mechanical polishing (CMP).

ADVANTAGE - Consistent density and distribution of active regions on one chip
can be obtained

CHOSEN-DRAWING: Dwg.1a/2

TITLE-TERMS:
CMP UNIFORM INCREASE METHOD OBTAIN CONSISTENT DENSITY
DISTRIBUTE ACTIVE REGION
ONE CHIP

DERWENT-CLASS: U11

EPI-CODES: U11-C06A1A;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N2001-044317

DOCUMENT-IDENTIFIER: US 6093631 A
TITLE: **Dummy patterns** for aluminum chemical polishing (CMP)

---------- KWIC ---------

APD:
19980115

TTL:
Dummy patterns for aluminum chemical polishing (CMP)

ABPL:
A method and apparatus is provided for planarizing damascene metallic circuit **patterns** of a plurality of discrete integrated circuit chips on a metal coated silicon wafer wherein the circuitry on the chips on the wafer are either designed to be within a defined high metal density circuit range and low density metal circuit range and/or to provide **dummy** circuitry in the damascene process to provide a substantially uniform circuit density over the chip and the wafer surface. It is preferred that each chip on the surface of the wafer be divided into a plurality of regions and that each region be provided with dummy metallization, if necessary, to provide a relatively uniform circuit density in that region and consequently on the wafer surface. The invention also contemplates adding dummy circuitry to the periphery of the wafer in areas which are not formed into chips (chip fragments). The invention also provides semiconductor wafers made using the method and/or apparatus of the invention.

BSPR:
One method for forming the interconnects is to use a damascene method wherein, in general, a via or trench pattern is etched into a planar **dielectric** layer

and then the pattern is filled by metal. Excess metal is typically applied and
covers the upper surface of **dielectric**. The excess metal is then polished away
to the patterned metal surface. As with other steps in the fabrication
process, it is of extreme importance that the polished interconnect damascene
layer be planar.

BSPR:
With regard to the semiconductor devices formed from the wafer, the devices
typically include a plurality of interlayered circuits such as metal lines
forming an integrated circuit which are interconnected by vias or interconnects
between the layers. In the damascene process, metallization of the
interconnects is performed by etching the desired circuitry in the **dielectric**
layer down to the active region of the device. A thin layer of conductive
metal is deposited by, for example, vacuum evaporation, sputtering or chemical
vapor deposition (CVD) techniques, over the entire

BSPR:
Both single damascene structures and double damascene layers may be made by the
same process and both processes require a CMP process to polish the wafer down
to the surface of the interconnects and provide a planar surface.
Unfortunately, problems such as dishing occur causing a non-planar surface.
The dishing effect is particularly serious since the polishing needs to be
carried out until the metal is cleared on the entire wafer, i.e., wherein the
metal is left exclusively in previously etched lines without any metal on the
surface of the **dielectric**. It has been found that a significant overpolish is
typically needed which results in erosion of **dielectric** and dishing of metal as
much as 100 nm below the level of the **dielectric** surface.

As a consequence,
the thickness of the interconnects in overpolished areas is severely reduced
resulting in an increased sheet resistance as compared to interconnects in
other areas of the wafer and/or the individual integrated circuit device.
Additionally, an uneven topography is introduced on the wafer surface after CMP
which will be repeated with slight attenuation after subsequent deposition of
dielectric layers problems at later steps in the fabrication process.

BSPR:
In areas of high pattern factor (HPF), e.g., 60% it has been found that the
metal surface, after deposition, is lower than in areas of low pattern factor
(LPF) areas, e.g., 20% due to mass conservation during the sputtering or other
deposition process. As a consequence, during the CMP process, the metal above
the **dielectric** is removed differently in HPF areas as compared to LPF areas.
Since the polishing needs to be carried out until the patterned metal is
cleared on the entire wafer leaving metal exclusively in previously etched
lines, HPF areas generally experience a significant overpolish resulting in
erosion of the **dielectric** and dishing of metal up to 100 nm below the level of
the **dielectric** surface. As a result, the thickness or height of lines
(interconnects) in HPF areas is thinner or shorter resulting in increased sheet
resistance as compared to the thicker lines in LPF areas.

BSPV:
forming both the desired circuit pattern and any dummy circuit pattern as
openings in a dielectric layer on each chip;

BSPV:
coating the patterned **dielectric** layer with a layer of metal which metal fills

the **openings** forming the desired circuit pattern and any **dummy** circuit pattern
and covers the surface of the wafer including the circuit **patterns**; and

BSPV:
polishing the metal coated wafer until no metal remains outside the desired and
any **dummy** circuit **patterns**.

DEPR:
Referring now to FIGS. 11A-11D, the method of the invention of adding dummy
metallization to a region of the chip is shown. In FIG. 11A, a silicon
substrate 13 is shown having a silicon dioxide **dielectric** layer 14 thereon. In
the **dielectric** layer 14 **openings** 15a, 15b, 15c and 15d are formed for
interconnect **openings** and extend from the surface of layer 14 to the surface of
silicon wafer 13. This configuration is similar to the configuration as shown
in FIG. 3A. FIG. 11B shows the addition of dummy lines 20 which are the same
as the addition of the dummy lines as shown in FIG. 3B. In FIG. 11C, a metal
layer 16 is coated on top of **dielectric** layer 14 filling the **openings** 15a-15d
and the dummy **openings** 20. The surfaces 16a and 16b of metal layer 16 at the
opposed sides of region 17 are shown as being substantially horizontal (planar)
indicating uniform metallization on the surface of region 17. The height of
the **openings in the dielectric** layer 14 is shown as h. The metallized wafer of
FIG. 11C is now chemical mechanically polished using conventional means to
remove metal layer 16 down to the surface of **dielectric** 14. It can be seen
that the remaining **dielectric** surface as indicated by opposed ends 14a and 14b
is substantially horizontal over the region 17 of the chip.

DEPR:
FIGS. 11A-11D showing the method of the invention using

dummy circuitry to
provide a uniform metallized **dielectric** surface is to be
contrasted with FIGS.
10A-10C which show a method of planarization of a damascene
layer of the prior
art. Thus, in FIG. 10A, a region 17 of the chip has a
silicon substrate 13 and
a **dielectric** layer 14 thereon. **Openings** having a height h
are provided in the
dielectric and are identified as 15a-15d. In FIG. 10B, a
metal layer 16 is
deposited on the surface of **dielectric** layer 14 filling the
openings 15a-15d
and covering the complete surface of the **dielectric**.
Because of the
conservation of mass, the metal 16 deposited on **dielectric**
surface 14 will be
uneven (non-planar) having a lower height shown as 16a
compared to a higher
level 16b. The lower level 16a is over the high pattern
factor area including
openings 15a, 15b and 15c as compared to the higher level
16b which is over a
lower pattern factor area including only opening 15d.

DEPR:
The wafer of FIG. 10B is then chemically-mechanically
polished resulting in
removal of metal layer 16 down to the **openings in**
dielectric layer 14. As can
be seen in FIG. 10C, the height h' of the high pattern
factor area shown as
having **openings** 15a, 15b and 15c is lower than the height h
of the low pattern
factor area which only has opening 15d therein.

DEPR:
The above description has been directed to silicon wafers
and the use of a
silicon dioxide as the **dielectric**. It will be appreciated
by those skilled in
the art that any wafer material and **dielectric** material may
suitably be used in
the method of the invention. Likewise, any metal may be
used to metallize the
damascene **openings** in the wafer surface with suitable

metals including
aluminum, copper, tungsten and the like. Typically, the thickness of the metal
layer above the surface of the **dielectric** is about 0.5 to 1 microns.

CLPR:
6. The method of claim 1 wherein **dummy** circuit **patterns** or the setting of a
maximum and/or minimum metal density are provided for chip fragments at the
edge of the wafer.

CLPV:
forming both the desired circuit pattern and any dummy circuit pattern as
openings in a dielectric layer on each chip;

CLPV:
coating the patterned **dielectric** layer with a layer of metal which metal fills
the **openings** forming the desired circuit pattern and any **dummy** circuit pattern
and covers the surface of the wafer including the circuit **patterns**; and

CLPV:
polishing the metal coated wafer until no metal remains outside the desired and
any **dummy** circuit **patterns**.